MERI College of Engineering & Technology (MERI-CET)

Lesson plan

Name of the faculty: Er. Gaurav Kumar

Discipline: ECE/EEE

Semester: 4th

Subject: Digital Electronics

Lesson Plan Duration: 16 weeks (From May, 2021 to Sep 2021)

Work Load (Lecture/ Practical) per week (in hours): Lecture-02, Practical-01

Week	Theory		Practical	
	Lecture day	Topic(Including assignment/test)	Practical Day	Topic
1st	1st	Introduction of Logic Simplification	1st	Introduction of Digital System Design Lab
	2nd	Review of Boolean Algebra		
2nd	1st	Review of DeMorgan's Theorem	2nd	To study & design basic gates
	2nd	SOP & POS forms		
3rd	1st	SOP & POS forms	3rd	To study & design basic gates
	2nd	Realization Using Gates. K- maps up to 6 variables		
4th	1st	K-maps up to 6 variables	4th	To realize and minimize five & six variables using K-Map method
	2nd	VEM technique		
5th	1st	Binary codes	5th	To verify the operation of Multiplexer & De-multiplexer
	2nd	Code Conversion Numerical.		
6th	1st	**Combinational & Sequential Logic Design**: Comparators	6th	To perform Half adder and Full adder
	2nd	Multiplexers		

7th	1st	Encoder, Decoder	7th	To perform Half adder and Full adder.	
	2nd	Driver & Multiplexed Display, Half and Full Adders, Subtractor.			
8th	1st	Parallel Adders, Adder with Look Ahead Carry ,BCD Adder	8th	To perform Half Substractor and Full subtractor	
	2nd	Sequential Logic Design: Building blocks like S-R			
9th	1st	JK and Master-Slave JK Flip Flop	9th	To verify the truth table of S-R,J-K,T & D Type flip flop	
	2nd	Ripple and Synchronous counters, Sequence Generator, Shift registers.			
10th	1st	**Finite state machines**: Introduction, Design of synchronous FSM	10th	To study FLIP- FLOP conversion.	
	2nd	Serial Binary Adder			
11th	1st	Sequence detector, Parity Bit Generator	11th	To design & verify the operation of a 3 bit synchronous counter.	
	2nd	Pulse train generator			
12th	1st	Algorithmic State Machines charts	12th	To design & verify the operation of synchronous UP/DOWN decade counter using JK flip	
	2nd	Introduction, Component of ASM chart			
13th	1st	Introductory examples of ASM chart.	13th	Conversion of state diagram to the state table and implement it using logical ckt.	
	2nd	**Introduction of Logic Families and PLDs**			
14th	1st	TTL NAND gate, Specifications	14th	Design a RLC resonance circuit & verify the transient response for different values of R, L & C	
	2nd	Noise margin, Propagation delay			
15th	1st	fan-in, fan-out	15th	Discussion of Previous Year Question Paper.	

	2nd	Tri State TTL, ECL, CMOS families and their interfacing		
16th	1st	Concept of Programmable logic devices like PAL, PLA,ROM,CPLD and FPGA.		
	2nd	Logic implementation using Programmable Devices.		

Text/Reference Books:

1. R.P. Jain, "Modern digital Electronics", Tata McGraw Hill, 4th edition, 2009
2. A.Anand Kumar, "Switching Theory & Logic Design",PHI.
3. W.H. Gothmann, "Digital Electronics- An introduction to theory and practice", PHI, 2nd edition ,2006.
4. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989.
5. Morris Mano, "Digital Design: With an Introduction to the Verilog HDL 5th Edition, Pearson Education, 2013.
6. Morris Mano, "Logic & Computer Fundamentals,4th Edition, Pearson Education.
7. A.V. Oppenheim, A.S. Willsky, with S. Nawaab "Signals & Systems"2nd Edition, Pearson Education, 2015.